REMARKS

This application has been reviewed in light of the Office Action dated May 3, 2006. Claims 1-30 are pending in the application. By the present amendment, claims 1, 13 and 22 have been amended. No new matter has been added. The Examiner's reconsideration of the rejection in view of the amendment and the following remarks is respectfully requested.

By the Office Action, claims 1-30 stand rejected under 35 U.S.C. §102 (b) as being anticipated by U.S. Patent No. 5,765, 035 to Tran (hereinafter Tran).

Tran is directed to a system having a reorder buffer that detects dependencies between accesses to caches. The reorder buffer compares memory accesses of after execution or issuance by decode/issue stage (208) to memory accesses from a decode stage. If the execution stage's read memory access is dependent on a write memory access performed by the decode stage, the read access is stalled until the write access completes. If the read depends on the write access the memory is flushed. Note that the reorder buffer receives the memory access of the execution stage. It is therefore, axiomatic the reorder buffer must be downstream from and receive issued instructions from the execution stage.

Claim 1 of the present invention, includes, *inter alia*, a pipeline including a plurality of operational stages, the stages include: a pointer register stage ... , a dependency checking stage located downstream of the pointer register stage, which determines if instruction dependencies exist and stalls an issue prior to issuance if necessary to resolve inter-instruction dependencies, at least one functional unit ... .

The present claims provide a dependency checking stage located downstream of the pointer register stage, which determines if instruction dependencies exist and stalls an issue prior to issuance if necessary to resolve inter-instruction dependencies. The dependency

checking stage is located before the issue stage but downstream of the pointer register stage (See FIG. 2 of the present application). In this way, an instruction is stopped before it is issued if dependencies exist which may have an impact of the output of the instruction.

Many advantages are provided in accordance with this methodology. For example, by applying the systems and methods of the present invention, greater flexibility is afforded to a programmer or pipeline designer, since instruction order and dependencies become less of an issue. This permits the focus of the programmer to shift to other problems or issues while still maintaining a high level of performance, even for codes where there is a high frequency of inter-instruction dependencies through the pointer registers. This high performance level is achieved by minimizing the number of stalls and/or unused instruction issue slots between such dependent instructions. The precise pointer file mechanism of the present invention permits the support of precise exceptions with low performance and hardware overhead.

Tran fails to disclose or suggest at least: a dependency checking stage located downstream of the pointer register stage, which determines if instruction dependencies exist and stalls an issue prior to issuance if necessary to resolve inter-instruction dependencies. The Examiner stated that reorder buffer 216 of Tran provides a dependency checking stage essentially as claims in the present application. While the reorder buffer does consider dependencies, this is performed after the issuance of a command. See FIG. 1 where issue stage 208 is upstream of the reorder buffer 216. According to Tran the instruction is executed first before reordering is performed. In accordance with the present claims, prior to issuance, dependencies are checked and instructions stalled to update the dependencies. This is not contemplated by Tran.

Therefore it is respectfully submitted that Tran fails to disclose or suggest all of the elements of claims 1, 13 and 22 as amended. Tran fails to disclose or suggest at least a dependency checking stage located downstream of the pointer register stage, which determines if instruction dependencies exist and stalls an issue prior to issuance if necessary to resolve inter-instruction dependencies. Claim 1, 13 and 22 are believed to be in condition for allowance for at least the stated reasons. Dependent claims 2-12, 14-21 and 23-30 are also believed to be allowable for at least their dependencies from claims 1, 13 and 22, respectively. Reconsideration of the rejection is earnestly solicited.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's IBM Deposit Account No. 50-0510.

Respectfully submitted,

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